Listing of Claims

11. (Currently Amended) A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon ~~oxide~~ substrate having a source/drain region;

a tunnel oxide layer disposed over said silicon substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

~~a sidewall forming~~ a single floating gate aligned to one side of said select gate;

a third insulated material ~~located directly on~~ contacted with said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material.

12. (Original) The structure according to Claim 11, wherein each of said first insulated material, said second insulated material and said third insulated material is one selected from a group consisting of silicon oxide, silicon nitride and silicon oxide/nitride composite.

13. (Original) The structure according to claim 11, wherein said conductive layer is one selected from a group consisting of polysilicon, amorphous silicon, recrystallized silicon and polycide.

14. (Original) The structure according to claim 11, wherein each of said floating gate and said control gate is one selected from a group consisting of polysilicon, amorphous silicon and recrystallized silicon.

15. (Currently Amended) A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon substrate having a source/drain region;

a tunnel oxide layer disposed over said silicon substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a floating gate aligned to one side of said select gate;

a third insulated material ~~located directly on~~ contacted with said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material, wherein said control gate partially covers said third insulated material.